

Abstract

5 A processing system comprising processors and the dynamically configurable
communication elements coupled together in an interspersed arrangement. The
processors each comprise at least one arithmetic logic unit, an instruction processing unit,
and a plurality of processor ports. The dynamically configurable communication
elements each comprise a plurality of communication ports, a first memory, and a routing
engine. For each of the processors, the plurality of processor ports is configured for
10 coupling to a first subset of the plurality of dynamically configurable communication
elements. For each of the dynamically configurable communication elements, the
plurality of communication ports comprises a first subset of communication ports
configured for coupling to a subset of the plurality of processors and a second subset of
communication ports configured for coupling to a second subset of the plurality of
15 dynamically configurable communication elements.

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